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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,325	12/29/2003	Colin Whitby-Strevens	APPL-P3015	1716

28661 7590 05/26/2006

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EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,325	WHITBY-STREVENS ET AL.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-28* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/6/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 28 have been examined.

Specification

The disclosure is objected to because of the following informalities: Paragraph 6, line 4 is missing a space between "symbol" and "into." Paragraph 6, line 12 contains a misspelling of the word "which" (see "with").

Appropriate correction is required.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Paragraph 23, line 6 contains reference signs 100 and 103 that are not shown in the drawings. Page 9, line 2 contains reference sign 107, which is not shown in the drawings. Paragraph 26 refers to reference sign 120, which is not shown in the drawings. Paragraph 34 refers to reference sign 230, which is not shown in the drawings. Paragraph 35 refers to reference sign 232, which is not shown in the drawings. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as

either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 26 is objected to because of the following informalities: claim 26, lines 5 – 6 contains the phrase "is be." Appropriate correction is required.

Claim 28 recites the limitation "the autonegotiation mechanism" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 25 is rejected under 35 U.S.C. 102(b) as being anticipated by Smith et al.

Regarding claim 25, Smith et al. teach an apparatus for transmitting data across a high-speed serial bus, the apparatus comprising:

An IEEE 802.3-compliant PHY having a GMII interface (column 5, lines 54 – 56; Figure 4, item 110);

An IEEE 1394-compliant PHY in communication with the IEEE 802.3-compliant PHY (Figure 4, item 108);

A first connection, the first connection for transmitting data between a device and the IEEE 802.3-compliant PHY (Figure 4, item 802.3 GMII Interface);

A second connection, the second connection for transmitting data between a device and the IEEE 1394-compliant PHY (Figure 4, item 1394 PHY-Link Interface).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. in view of Crutchfield et al.

Regarding claim 1, Smith et al. teach a method of transmitting data across a high-speed serial bus, the method comprising:

In accordance with a first TX symbol clock (Figure 5, item SCLK50M);

Generating a symbol on an IEEE 1394-compliant PHY having a port interface (column 6, lines 31 – 33; Figure 4, item 1394 PHY-Link Interface);

Placing the symbol on the port interface (column 6, lines 21 – 30);

Placing the symbol in a FIFO (column 6, lines 37 – 40);

In accordance with a second TX clock, the second TX clock running at a different speed than the first TX clock (column 7, lines 1 – 2);

Rèmoving the symbol from the FIFO (Examiner notes that, consistent with the operation of a FIFO, in order for the data to move from Figure 5, item 204, to 206, as indicated by the arrows, the symbol would have to be removed from the FIFO);

Sending the 8-bit byte to an IEEE 802.3-compliant PHY (column 6, lines 14 – 16; Figure 4, item 110; Examiner notes that the symbol would have to be an 8-bit byte since the IEEE 802.3-compliant PHY only supports 8-bit data transfers);

Smith et al. fail to teach generating a 10-bit symbol, scrambling the 10-bit symbol, encoding the 10-bit symbol, and deriving an 8-bit byte from the removed 10-bit symbol.

Crutchfield et al. teach sending a 10-bit signal on an IEEE 1394 bus, scrambling the symbol, encoding it, and transmitting it on the bus to the destination where it is decoded into an 8-bit word for the purpose of reducing radiated emissions, and providing DC balance and clock recovery (paragraphs 12, 13). These advantages help to make the method of transmitting data across a high-speed serial bus more reliable.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the method of sending a 10-bit signal as taught by Crutchfield et al. into the method of Smith et al. for the purpose of making the method of transmitting data across a high-speed serial bus more reliable.

Regarding claim 2, Smith et al. and Crutchfield et al., fail to explicitly teach wherein a symbol is removed from the FIFO on four out of every five GMII TX clock cycles. Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to remove a symbol from the FIFO on every GMII TX clock cycle in order for processing to continue. Removing a symbol on every clock cycle would include removing a symbol on four out of every 5 GMII TX clock cycles, and therefore meets this limitation.

Regarding claim 3, Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to place a null symbol in the FIFO when no symbols were present to indicate that the FIFO were empty. This is evidenced by D'Ignazio et al. in column 4, lines 50 – 54.

* * *

Claims 4 - 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. in view of Crutchfield et al., and further in view of Thayer et al.

Regarding claim 4, Smith et al. teach a FIFO (column 6, lines 37 – 40) but fail to teach wherein the 8-bit byte is derived from the 10-bit symbol by using 8 bits from the extracted 10-bit symbol, and the two remaining bits are stored.

Thayer et al. teach a method of data alignment when transferring data between devices of differing widths for the purpose of improving performance (column 1, lines 12 – 16; column 2, lines 10 – 19; Figures 11A – 11G). Examiner notes that while Thayer et al. does not expressly teach deriving an 8-bit byte from a 10-bit symbol, they do show, for example, how two 16-bit symbols may be derived from a single 24-bit symbol. Examiner notes that these figures (Figures 11A – 11G) would provide sufficient teaching for one of ordinary skill in this art to develop other varying-bit symbol permutations.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the data alignment as taught by Thayer et al. into the method of Smith et al. and Crutchfield et al. for the purpose of improving performance.

Claims 5 – 8 follow similar methodology as claim 4 and are rejected using the same rationale as above.

Regarding claim 9, Smith et al. teach the additional limitation comprising in accordance with a phase amplitude modulation clock, sending the received 8-bit byte from the IEEE 802.3-compliant PHY to a device in accordance with a phase amplitude modulation clock (column 7, lines 1 – 2).

* * *

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. in view of Crutchfield et al., in view of Thayer et al., and further in view of Anderson et al.

Regarding claim 10, Smith et al. teach a method of transmitting data across a highi-speed serial bus, the method comprising:

Receiving an 8-bit byte (column 6, lines 14 – 16; Figure 4, item 110; Examiner notes that the symbol would have to be an 8-bit byte since the IEEE 802.3-compliant PHY only supports 8-bit data transfers);

In accordance with a GMII RX clock (Figure 5, item RCLK);

If the received 8-bit byte contains a null symbol, then deleting the null symbol (Examiner takes official notice that it is old, and well known in the art to remove data padding upon receiving a piece of data for processing. White et al. evidence this in column 2, lines 16 – 20, column 4, lines 1 – 4, and Figure 6. Additionally, Smith teaches padding and stripping data with checksums (column 6, lines 21 - 29).

Else, storing the 8-bit byte in a register (Examiner takes official notice that a FIFO may be implemented using registers, as evidenced by Kohn in column 7, lines 8 – 10; Smith et al.: column 6, lines 37 – 40; Figure 5, item 210);

Receiving a second 8-bit byte that does not contain a null symbol and storing the second 8-bit byte in a second register (Examiner takes official notice that a FIFO may

be implemented using multiple registers, as evidenced by Kohn in column 7, lines 8 – 10; Smith et al.: column 6, lines 37 – 40; Figure 5, item 210);

Smith et al. teach a FIFO (which may be implemented using registers) (column 6, lines 37 – 40) but fail to teach assembling a 10-bit symbol from the 8-bit byte stored in the first register and appending two bits from the 8-bit byte stored in the second register.

Thayer et al. teach a method of data alignment when transferring data between devices of differing widths for the purpose of improving performance (column 1, lines 12 – 16; column 2, lines 10 – 19; Figures 11A – 11G). Examiner notes that while Thayer et al. does not expressly teach deriving assembling a 10-bit symbol from an 8-bit byte stored in a first register and 2 bits in a second register, they do show, for example, how two a 24-bit symbol can be assembled from 3 8-bit symbols (Figure 11D). Examiner notes that these figures (Figures 11A – 11G) would provide sufficient teaching for one of ordinary skill in this art to develop other permutations of the same method.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the data alignment as taught by Thayer et al. into the method of Smith et al. and Crutchfield et al. for the purpose of improving performance.

Smith et al. teach placing the symbol in a FIFO (Figure 5, item 210; column 6, lines 37 – 40), in accordance with a second clock (Figure 5, item SCLK50M, removing the 10-bit symbol from the first FIFO (Examiner notes that, consistent with the operation of a FIFO, in order for the data to move from Figure 5, item 210, to 212, as indicated by the arrows, the symbol would have to be removed from the FIFO) and sending the

decoded 10-bit symbol to an IEEE 1394 compliant PHY (Figure 5, item 202; column 6, lines 31 – 33).

Smith et al. fail to teach flagged decoding on the assembled 10-bit symbol.

Crutchfield et al. teach receiving a 10-bit signal on an IEEE 1394 bus, and performing 8B10B and control decoding it for the purpose of reducing radiated emissions, and providing DC balance and clock recovery (paragraphs 12, 13). These advantages help to make the method of transmitting data across a high-speed serial bus more reliable.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the method of sending a 10-bit signal as taught by Crutchfield et al. into the method of Smith et al. for the purpose of making the method of transmitting data across a high-speed serial bus more reliable.

Smith et al, Crutchfield et al., and Thayer et al. fail to teach placing the decoded 10-bit signal into a second FIFO in accordance with a third clock, removing the decoded 10-bit symbol from the second FIFO and sending the decoded 10-bit symbol to an IEEE 1394-compliant PHY.

Anderson et al. teach placing the symbol in a second FIFO (Figure 1, item 5);

In accordance with a third clock (column 7, lines 64 – 66):

Removing the decoded symbol from the second FIFO (column 9, lines 13 – 15);

Sending the decoded symbol to an IEEE 1394-compliant PHY (Figure 1, item 2).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the method of Anderson et al. into the

method of Smith et al, Crutchfield et al., and Thayer et al. for the purpose of maximizing the opportunity to successfully transmit useful information within an allocated time (column 6, lines 38 – 41. This would have been obvious in order to improve the performance of the system.

* * *

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. in view of Crutchfield et al., in view of Thayer et al., in view of Anderson et al., and further in view of Voit.

Regarding claim 11, Smith et al., Crutchfield et al., Thayer et al., and Anderson et al. fail to teach wherein the second clock is phase locked to the third clock.

Voit teaches phase locking different clock signals together in order to reduce setup and hold times associated with the components (column 5, lines 45 – 65).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to phase lock, as taught by Voit, the second and third clocks of Smith et al., Crutchfield et al., Thayer et al., and Anderson et al., for the purpose of reducing setup and hold times within the system, thereby improving system performance.

* * *

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. in view of Crutchfield et al.

Regarding claim 13, Smith et al. teach a method of transmitting data across a high-speed serial bus, the method comprising:

In accordance with a first TX symbol clock (Figure 5, item SCLK50M);

Generating a symbol on an IEEE 1394-compliant PHY having a port interface (column 6, lines 31 – 33; Figure 4, item 1394 PHY-Link Interface);

Placing the symbol on the port interface (column 6, lines 21 – 30);

Placing the symbol in a FIFO (column 6, lines 37 – 40);

In accordance with a second TX clock, the second TX clock running at a different speed than the first TX clock (column 7, lines 1 – 2);

Removing the symbol from the FIFO (Examiner notes that, consistent with the operation of a FIFO, in order for the data to move from Figure 5, item 204, to 206, as indicated by the arrows, the symbol would have to be removed from the FIFO);

Sending the 8-bit byte to an IEEE 802.3-compliant PHY (column 6, lines 14 – 16; Figure 4, item 110; Examiner notes that the symbol would have to be an 8-bit byte since the IEEE 802.3-compliant PHY only supports 8-bit data transfers);

Smith et al. fail to teach generating a 10-bit symbol, flagged encoding the 10-bit symbol, and deriving an 8-bit byte from the removed 10-bit symbol.

Crutchfield et al. teach sending a 10-bit signal on an IEEE 1394 bus, flagged encoding the symbol, and transmitting it on the bus to the destination where it is decoded into an 8-bit word for the purpose of reducing radiated emissions, and

providing DC balance and clock recovery (paragraphs 12, 13). These advantages help to make the method of transmitting data across a high-speed serial bus more reliable.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the method of sending a 10-bit signal as taught by Crutchfield et al. into the method of Smith et al. for the purpose of making the method of transmitting data across a high-speed serial bus more reliable.

Regarding claim 14, Smith et al. and Crutchfield et al., fail to explicitly teach wherein a symbol is removed from the FIFO on four out of every five GMII TX clock cycles. Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to remove a symbol from the FIFO on every GMII TX clock cycle in order for processing to continue. Removing a symbol on every clock cycle would include removing a symbol on four out of every 5 GMII TX clock cycles, and therefore meets this limitation.

Regarding claim 15, Examiner takes official notice that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to place a null symbol in the FIFO when no symbols were present to indicate that the FIFO were empty. This is evidenced by D'Ignazio et al. in column 4, lines 50 – 54.

* * *

Claims 16 - 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. in view of Crutchfield et al., and further in view of Thayer et al.

Regarding claim 16, Smith et al. teach a FIFO (column 6, lines 37 – 40) but fail to teach wherein the 8-bit byte is derived from the 10-bit symbol by using 8 bits from the extracted 10-bit symbol, and the two remaining bits are stored.

Thayer et al. teach a method of data alignment when transferring data between devices of differing widths for the purpose of improving performance (column 1, lines 12 – 16; column 2, lines 10 – 19; Figures 11A – 11G). Examiner notes that while Thayer et al. does not expressly teach deriving an 8-bit byte from a 10-bit symbol, they do show, for example, how two 16-bit symbols may be derived from a single 24-bit symbol. Examiner notes that these figures (Figures 11A – 11G) would provide sufficient teaching for one of ordinary skill in this art to develop other permutations of the same method.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the data alignment as taught by Thayer et al. into the method of Smith et al. and Crutchfield et al. for the purpose of improving performance.

Claims 17 – 20 follow similar methodology as claim 4 and are rejected using the same rationale as above.

Regarding claim 21, Smith et al. teach the additional limitation comprising in accordance with a phase amplitude modulation clock, sending the received 8-bit byte

from the IEEE 802.3-compliant PHY to a device in accordance with a phase amplitude modulation clock (column 7, lines 1 – 2).

* * *

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. in view of Crutchfield et al., and further in view of Thayer et al.

Regarding claim 22, Smith et al. teach a method of transmitting data across a highi-speed serial bus, the method comprising:

Receiving an 8-bit byte on an IEEE 802.3-compliant PHY (column 6, lines 14 – 16; Figure 4, item 110; Examiner notes that the symbol would have to be an 8-bit byte since the IEEE 802.3-compliant PHY only supports 8-bit data transfers);

In accordance with a GMII RX clock (Figure 5, item RCLK);

If the received 8-bit byte contains a null symbol, then deleting the null symbol (Examiner takes official notice that it is old, and well known in the art to remove data padding upon receiving a piece of data for processing. White et al. evidence this in column 2, lines 16 – 20, column 4, lines 1 – 4, and Figure 6. Additionally, Smith teaches padding and stripping data with checksums (column 6, lines 21 - 29).

Storing the 8-bit byte in a register (Examiner takes official notice that a FIFO may be implemented using registers, as evidenced by Kohn in column 7, lines 8 – 10; Smith et al.: column 6, lines 37 – 40; Figure 5, item 210);

Receiving a second 8-bit byte that does not contain a null symbol and storing the second 8-bit byte in a second register (Examiner takes official notice that a FIFO may be implemented using multiple registers, as evidenced by Kohn in column 7, lines 8 – 10; Smith et al.: column 6, lines 37 – 40; Figure 5, item 210);

Smith et al. teach a FIFO (which may be implemented using registers) (column 6, lines 37 – 40) but fail to teach assembling a 10-bit symbol from the 8-bit byte stored in the first register and appending two bits from the 8-bit byte stored in the second register.

Thayer et al. teach a method of data alignment when transferring data between devices of differing widths for the purpose of improving performance (column 1, lines 12 – 16; column 2, lines 10 – 19; Figures 11A – 11G). Examiner notes that while Thayer et al. does not expressly teach deriving assembling a 10-bit symbol from an 8-bit byte stored in a first register and 2 bits in a second register, they do show, for example, how two a 24-bit symbol can be assembled from 3 8-bit symbols (Figure 11D). Examiner notes that these figures (Figures 11A – 11G) would provide sufficient teaching for one of ordinary skill in this art to develop other permutations of the same method.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the data alignment as taught by Thayer et al. into the method of Smith et al. and Crutchfield et al. for the purpose of improving performance.

Smith et al. teach placing the symbol in a FIFO (Figure 5, item 210; column 6, lines 37 – 40), in accordance with a second clock (Figure 5, item SCLK50M, removing the 10-bit symbol from the first FIFO (Examiner notes that, consistent with the operation

of a FIFO, in order for the data to move from Figure 5, item 210, to 212, as indicated by the arrows, the symbol would have to be removed from the FIFO) and sending the decoded 10-bit symbol to an IEEE 1394 compliant PHY (Figure 5, item 202; column 6, lines 31 – 33).

Smith et al. fail to teach flagged decoding on the assembled 10-bit symbol.

Crutchfield et al. teach receiving a 10-bit signal on an IEEE 1394 bus, and decoding it for the purpose of reducing radiated emissions, and providing DC balance and clock recovery (paragraphs 12, 13). These advantages help to make the method of transmitting data across a high-speed serial bus more reliable.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the method of sending a 10-bit signal as taught by Crutchfield et al. into the method of Smith et al. for the purpose of making the method of transmitting data across a high-speed serial bus more reliable.

Regarding claim 23, Smith et al. inherently teach wherein a received data valid state is asserted on the IEEE 802.3-compliant PHY since IEEE 802.3 inherently contains a receive data valid state as described in the IEEE 802.3 specification, page 17, section 22.2.2.6.

Regarding claim 24, Smith et al. teach wherein the FIFO compensates for ppm differences between the IEEE 802.3-compliant PHY and the IEEE 1394-compliant PHY

(Column 2, lines 45 – 50 teach that speed compensating is done via a padding algorithm. Column 6, lines 23 –24 teach that Figure 6, item 204 is a padding unit. Column 6, lines 37 – 40 teach that Figure 6, item 204 contains a FIFO. Therefore, the FIFO is, at least in part, responsible for the data padding, which is responsible for speed compensation between the IEEE 802.3-compliant PHY and IEEE 1394-compliant PHY.).

* * *

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. in view of Tatum et al.

Regarding claim 26, Stone et al. teach an apparatus for transmitting data across a high-speed serial bus, the apparatus comprising:

An IEEE 802.3-compliant PHY (Figure 5, item 122);

An IEEE 1394-compliant PHY in communication with the IEEE 802.3-compliant PHY via a switch (Figure 5, items 134); the switch determining whether data transmission is to be routed to the IEEE 802.3-compliant PHY or the IEEE 1394-compliant PHY;

A first connection, the first connection for transmitting data between a device and the IEEE 802.3-compliant PHY (Figure 5, item 38);

A second connection, the second connection for transmitting data between a device and the IEEE 1394-compliant PHY (Figure 5, item 36).

Stone et al. fail to teach the IEEE 802.3-compliant PHY having a GMII interface.

Tatum et al. teach using a GMII interface for the purpose of providing high speed data transfer with low cost of implementation and maintenance, in addition to being compatible with previous Ethernet standards (column 2, lines 6 – 26).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate a GMII interface as taught by Tatum et al. into the apparatus of Stone et al. for purpose of providing high speed data transfer with low cost of implementation and maintenance, in addition to being compatible with previous Ethernet standards. This would have been obvious to improve the performance of the system.

Regarding claim 27, Stone et al. teach the additional limitation comprising an autonegotiation mechanism, the autonegotiation mechanism determining whether data is to be routed between the IEEE 802.3-compliant PHY and the IEEE 1394-compliant PHY (paragraph 14; Figure 5, item 134; where the autonegotiation mechanism controls the demultiplexer (134)).

Regarding claim 28, Stone et al. teach the additional limitation wherein the autonegotiation mechanism determines whether data is to be routed through the IEEE 802.3-compliant PHY (Figure 5, item 122) to the first connection (Figure 5, item 36; paragraph 14).

Allowable Subject Matter

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record neither teaches nor suggests all of the claimed subject matter of claim 12, including "**wherein frequency of null character deletion is used to control a phased locked loop, the phase locked loop associated with the second clock.**"

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDS

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100